Amendments to the Claims:

Please amend the claims as indicated.

1. (Currently Amended) An apparatus for managing errors in prefetched data, the apparatus comprising:

a prefetch module comprising executable code stored on a storage device, executed by a processor, and configured to prefetch a data packet from a first location into a second location in anticipation of receiving a request for the prefetched data packet and prior to receiving the request;

a validation module comprising executable code stored on the storage device, executed by the processor, and configured to correct single bit errors in the prefetched data packet, determine that the prefetched data packet contains an uncorrectable error, and store a first location address for the prefetched data packet with the uncorrectable error, wherein the address is stored in the second location and no address is stored for prefetched data packets without uncorrectable errors;

an identification module comprising executable code stored on the storage device, executed by the processor, and configured to associate an identifier with the prefetched data packet prior to receiving the request if the prefetched data packet contains the uncorrectable error, wherein the identifier is stored in the second location with the prefetched data packet;

a transfer module comprising executable code stored on the storage device, executed by the processor, and configured to transfer the prefetched data packet from the second location if the request is received;

an error recovery module comprising executable code stored on the storage device, executed by the processor, and configured to selectively initiate an error recovery process for the transferred prefetched data packet that has been determined to contain an uncorrectable error if the identifier is associated with the prefetched data packet by setting a flag; and

the validation module is further configured to signal an interrupt to initiate the error recovery process in response to the set flag, wherein the error recovery process comprises re-retrieving the data packet from the first location using the address.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Previously Presented) An apparatus for managing errors in prefetched data, the apparatus comprising:

a request module configured to request a transfer of a data packet from a first location by way of a communication bus;

a data transfer interface configured to prefetch the data packet from the first location into a second location in anticipation of receiving a request from the request module for the prefetched data packet and prior to receiving the request and transferring the data to the request module across the communication bus, the data transfer interface further configured to correct single bit errors in the prefetched data packet, determine that the prefetched data packet contains an uncorrectable error, store a first location address for the prefetched data packet with the uncorrectable error, wherein the address is stored in the second location and no address is stored for prefetched data packets without uncorrectable errors, associate an identifier with the prefetched data packet prior to receiving the request if the prefetched data packet contains the uncorrectable error, store the identifier in the second location with the prefetched data packet, to selectively initiate an error recovery process for the prefetched data packet if the prefetched data packet is transferred to the request module and the identifier is associated with the prefetched data packet by setting a flag, and signaling an interrupt to initiate the error recovery process in response to the set flag, wherein the error recovery process comprises re-retrieving the data packet from the first location using the address.

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Currently Amended) A system for managing errors in prefetched data, comprising:

a memory interface module comprising executable code stored on a storage device, executed by a processor, and configured to prefetch a data packet from a memory array to a temporary buffer in anticipation of receiving a request for the prefetched data packet and prior to receiving the request;

a validation module comprising executable code stored on the storage device, executed by the processor, and in communication with the memory interface module, the validation module configured to correct single bit errors in the prefetched data packet, determine whether the prefetched data packet contains an uncorrectable error, and store a memory array address for the prefetched data packet with the uncorrectable error, wherein the address is stored in the temporary buffer and no address is stored for prefetched data packets without uncorrectable errors;

an identification module comprising executable code stored on the storage device, executed by the processor, and configured to associate an identifier with

the prefetched data packet prior to receiving the request if the prefetched data packet contains the uncorrectable error, wherein the identifier is stored in the temporary buffer with the prefetched data packet;

a communication module comprising executable code stored on the storage device, executed by the processor, and in communication with the temporary buffer, the communication module configured to transmit the prefetched data packet from the temporary buffer across a communication bus to a requesting device if the request is received;

an error recovery module comprising executable code stored on the storage device, executed by the processor, and in communication with the communication module, the error recovery module configured to selectively initiate an error recovery process for the prefetched data packet by setting a flag if the identifier is associated with the prefetched data packet and the prefetched data packet has been transmitted by the communication module; and

the validation module is further configured to signal an interrupt to initiate the error recovery process in response to the set flag, wherein the error recovery process comprises re-retrieving the data packet from the memory array using the address.

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Previously Presented) A method for managing errors in prefetched data, the method comprising:

prefetching a data packet from a first location into a second location in anticipation of receiving a request for the prefetched data packet and prior to receiving the request;

correcting single bit errors in the prefetched data packet;

determining that the prefetched data packet contains at least one uncorrectable error;

storing a first location address for the prefetched data packet with the uncorrectable error, wherein the address is stored in the second location and no address is stored for prefetched data packets without uncorrectable errors;

associating an identifier with the prefetched data packet prior to receiving the request if the prefetched data packet contains the at least one uncorrectable error, wherein the identifier is stored in the second location with the prefetched data packet;

determining that the prefetched data packet in the second location has been transmitted for an intended use in response to the request;

selectively initiating an error recovery process only for the prefetched data packet by setting a flag if the identifier is associated with the prefetched data packet and the prefetched data packet has been transmitted for an intended use; and

signaling an interrupt to initiate the error recovery process in response to the set flag, wherein the error recovery process comprises re-retrieving the data packet from the first location using the address.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Currently Amended) An apparatus for managing errors in prefetched data, comprising:

means for prefetching a data packet from a first location into a second location in anticipation of receiving a request for the prefetched data packet and prior to receiving the request, the prefetching means comprising executable code stored on a storage device and executed by a processor;

means for correcting single bit errors in the prefetched data packet, the correcting means comprising executable code stored on the storage device and executed by the processor;

means for determining that the prefetched data packet contains at least one uncorrectable error, the error determining means comprising executable code stored on the storage device and executed by the processor;

means for storing a first location address for the prefetched data packet with the uncorrectable error, wherein the address is stored in the second location and no address is stored for prefetched data packets without uncorrectable errors, the storing means comprising executable code stored on the storage device and executed by the processor;

means for associating an identifier with the prefetched data packet prior to receiving the request if the prefetched data packet contains the at least one uncorrectable error, wherein the identifier is stored in the second location with the prefetched data packet, the associating means comprising executable code stored on the storage device and executed by the processor;

means for determining that the prefetched data packet in the second location has been transmitted for an intended use in response to the request, the packet determining means comprising executable code stored on the storage device and executed by the processor; and

means for selectively initiating an error recovery process only for the prefetched data packet by setting a flag if the identifier is associated with the prefetched data packet and the prefetched data packet has been transmitted for an intended use, the initiating means comprising executable code stored on the storage device and executed by the processor; and

means for signaling an interrupt to initiate the error recovery process in response to the set flag, wherein the error recovery process comprises re-retrieving the data packet from the first location using the address, the signaling means comprising executable code stored on the storage device and executed by the processor.

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Previously Presented) An article of manufacture comprising a program storage medium readable by a processor and embodying one or more instructions executable by a processor to perform a method for managing errors in prefetched data, the method comprising:

prefetching a data packet from a first location into a second location in anticipation of receiving a request for the prefetched data packet and prior to receiving the request;

correcting single bit errors in the prefetched data packet;

determining that the prefetched data packet contains at least one uncorrectable error;

storing a first location address for the prefetched data packet with the uncorrectable error, wherein the address is stored in the second location and no address is stored for prefetched data packets without uncorrectable errors;

associating an identifier with the prefetched data packet prior to receiving the request if the prefetched data packet contains the at least one uncorrectable error, wherein the identifier is stored in the second location with the prefetched data packet;

determining that the prefetched data packet in the second location has been transmitted for an intended use in response to the request; and

selectively initiating an error recovery process for the prefetched data packet by setting a flag if the identifier is associated with the prefetched data packet and the prefetched data packet has been transmitted for an intended use; and

signaling an interrupt to initiate the error recovery process in response to the set flag, wherein the error recovery process comprises re-retrieving the data packet from the first location using the address.

28. (Canceled)

29. (Canceled)

30. (Canceled)

31. (Canceled)

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (Canceled)

36. (Canceled)